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STATE-OF-THE ART OF MMIC TECHNOLOGY AND DESIGN IN WEST GERMANY

E. Pettenpaul

Siemens AG, Components Group, D-8000 Munich, FRG

Abstract

The report presents advanced CAD models of lumped element MMIC's and some new technological features - a selfaligned gate process called DIOM, and the successful application of x-ray lithography. Different types of amplifier MMIC's and devices for DBS and PAR will be discussed.

Introduction

There are mainly two national resources of GaAs microwave technique since more than 10 years. The first is H. Beneking's Semiconductor Institute at the university of Aachen, delivering numerous device and application orientated fundamental ideas, and the second are Siemens Research Laboratories and Components Group in Munich, where the design and realization of GaAs MMIC's is a major goal since 1978. A third important acitvity is the microwave CAD work of R.H. Jansen and I. Wolff at the university of Duisburg. Besides, new facilities are currently installed or extended at the national funded Fraunhofer and Max Planck Institutes.
The object of the present report is to discuss some specific aspects of a European Community funded CAD-project of Analog MMIC's, the introduction of two unique technological features, i.e. the selfaligned (SA) DIOM wafer process and x-ray lithographie (XRL), and finally to present an overview of the MMIC's being under investigation.

CAD tools

In most cases our MMIC design is done with a commercially available microwave CAD program called CADEC+, which is supplied by MCAD software, Aachen. But this CAD package is completed by several inhouse programs, among those is an advanced model description of passive lumped elements for MMIC's up to 18 GHz (1). The reason is that lumped elements are considered as very attractive structures due to the considerable size reduction.
The advanced models for the different lumped element structures were derived by the rigorous application of stripline theory in order to determine precise element values and losses, i.e. the designation "lumped" is only correct with respect to the selected dimensions (smaller than 0.1 wavelength). A specific feature is that straight line and single-loop inductors were sumulated by the solution of the inductor integral.
The proceeding of modeling the complex structures - circular or rectangular spiral inductors, and interdigitated capacitors - is similar: the structure is divided into its basic subcomponents, which are simulated separately and again put together by means of network theory. Thus the circular spiral inductor is separated in different single-loop inductors and the overall inductance value is calculated as the sum of each turns self and mutual inductance. Ground metallization is considered by a mirror spiral just as parasitic capacitances between turns via substrate, air and ground. In the case of the rectangular spiral inductor and interdigitated capacitor the subcomponents are single and coupled microstrip lines and bends, the microstrip open end, the unsymmetrical gap, and the microstrip T-junction.
The experimental verification of all models with extensive scaling investigations and improved test procedures using the resonant frequency shift method resulted in standard design rules for the layout, definition of a useful value and frequency range, and identification of the losses (1). Table 1 summarizes these results and gives additional information of the

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available model accuracy (test set-up losses are subtracted). The main message is that lumped elements, besides multi-turn inductors, can be applied beyond x-band, that the model accuracy even for very small elements is high, but the Q-factors of a convenient MMIC layout are below 100.
The present MESFET description uses in principal the exemplary lumped element equivalent circuit (e.c.) model proposed by P. Wolf. But in this work we applied a broadband approach, in which the inner FET is isolated from the extrinsic elements by deembedding and the e.c. elements are derived from small-signal s-parameters by a subsequent splitting of the different e.c. branches (2,3). An extensive experimental verification, including the tolerance behaviour in the range of the process induced standard deviations, showed that the models are valid up to 16 GHz with high accuracy.

Element	Useful MMIC values	Q 2 12 18 GHz	Dev. Exp / CAD %
Spiral Inductor	L = 1 - 5 nH	12 30 -	< ± 5
Single-Loop Inductor	L = 0.2 - 0.5 nH	12 30 35	< ± 10
Straight Line Inductor	L = 0.05 - 0.2 nH	18 40 50	< + 10
Interdigital Capacitor	C = 0.1 - 0.6 pF	50 50	≤ ± 5
	C = 0.02 - 0.05pF		< + 10
MIM-Capacitor	C = 0.5 - 20 pF	65 65	≤ ± 5

Table 1: CAD of Passive Lumped Elements, f = 1 - 18 GHz

MMIC Technology

The technology used for the fabrication of monolithic integrated circuits is a planar porcess with directly selective ion implantation (DSI^2), which is described in (4). Progresses in our device technology are mainly expected from three aspects:
- The introduction of a SA gate processing technique called DIOM (5,6),
- the application of XRL to subhalfmicron (SHM) gates (7,8),
- and the use of airbridge and via hole interconnection technologies.

The SA GaAs Schottky device fabrication process has been designated DIOM, an acronym for double Ge/Si contact implantation, one metallization. This abbreviation explains already the main two modified process steps, Fig. 1:
the Ohmic contact regions are doped using an additional high dose of Ge^+ besides the usual Si^+ implant, and thus allowing a single metallization step (Cr-Au-W-Au) for the Ohmic contacts and Schottky barriers. A deeper understanding of the amphoteric behaviour of the dopant germanium and the behaviour of the different metal layers after aging are given in (9).
The advantages of the SA DIOM wafer fabrication technique are process and device specific. Process simplicity and improved yield are a result of the single metallization step, a renunciation of an individual wafer gate recess, and a truly planar submicron (gate) lithography with the gate deposited symmetrically between the metallic source and drain electrodes. Compared to the SA techniques for digital IC's like the refractory metal gate technology developed in the Fujitsu laboratories (10) and NTT's dummy gate technology called SAINT (11), the DIOM process is not selfaligning with respect to the gate/n^+-layer but to the gate/Ohmic contacts. Moreover the DIOM process reveals no Schottky barrier degradation and promises SHM dimension capability as a smooth process with low gate metal resistance. Finally the DIOM MESFET showed improved uniformity with a standard deviation below 5 % for the dc and rf parameters, and very good temperature stability, i.e. dc delta-parameters below 5 % after 168 h burn-in at 200 °C channel temperature.
A unique possibility is used by the German cooperative for XRL with the Berlin Storage Synchroton ring (BESSY). This facility described in (12) is under control of the Fraunhofer Institute for Microstructure Technique, which is also responsible for the very difficult manufacture of the x-ray masks, consisting of a 2 µm thick silicon membrane with 1 µm thick galvanic gold absorber (13). Alignement is done with the x-ray stepper MAX 1 of Karl Suess KG, FRG.
The most attractive feature of XRL compared to e-beam lithography is the large-volume capability due to the highly parallel and intense x-ray source. This allows a one-to-one transfer of the mask structure to the wafer with a proximity distance mask-wafer of 50 µm and minimum (Fresnel) scattering effects. The exposure field currently used is 26.5 x 26.5 mm and will be increased step by step.
These XRL-facilities mainly installed for the fabrication of silicon VLSI RAM circuits were used to demonstate for the first time SHM metal line lithography feasibility. GaAs MESFET's with 0.45 µm gate length have been realized by F. Ponse et al. (7,8) using three layer PMMA and lift-off technique. A noise figure of 2 dB with 8 to 9 dB associated gain at 12 GHz was measured for the first devices although the evaporated gate metal had

only a thickness of 0.5 um. Improved SHM T-gates with smaller length and a thicker metal system are under investigation.

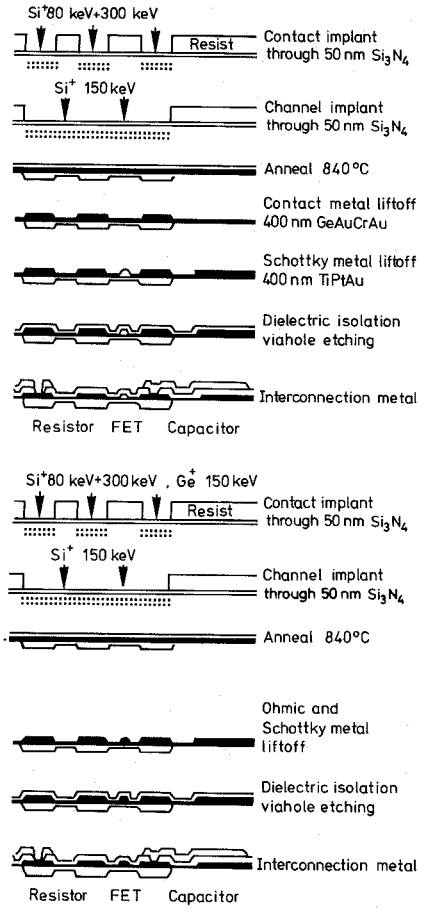

Fig. 1: Cross-sectional view of planar (DSI) and DIOM wafer process

Monolithic Analog IC's

The application potential of our analog IC's is in communication systems via radio link starting with the 140 MHz band, mobile radio communication at 450 or 900 MHz, direct broadcasting systems via satellite (12 GHz DBS in Europe), repeaters for coaxial and fiberoptic systems and of course in active phased array radar (PAR) receive systems up to x-band.

Our main emphasis is directed to a deeper understanding of the four in principal different amplifier types:

- the low-noise broad-band feedback amplifier,
- the low-noise matched amplifier with about 10 % bandwidth,
- the extremely broad-band distributed amplifier,
- and the high-gain differential amplifier

Circuit design and performance will be compared in this report. Besides, the development of a convenient dual-gate MESFET mixer will be described.

A different set of MMIC's is necessary for the receive path of an x-band PAR. Some principal features of SPDT FET switches, switched line phase shifters and attenuators shall be discussed.
An important precondition of MMIC's are the realization of low-loss, broad-band passive circuits on small chip size. The report will present first results on monolithic filters, matching networks and couplers in the 1 - 18 GHz range (14).

To give an example of the realized MMIC's, Fig. 2 and 3 show a chip SEM of lumped element feedback and matched amplifiers, respectively.

Conclusion

A high accuracy description of lumped elements for MMIC's is presented. Besides, the successful application of a self-aligned gate process together with the first realization of MESFET's in x-ray lithography is reported. An overview of the realized MMIC's is given.

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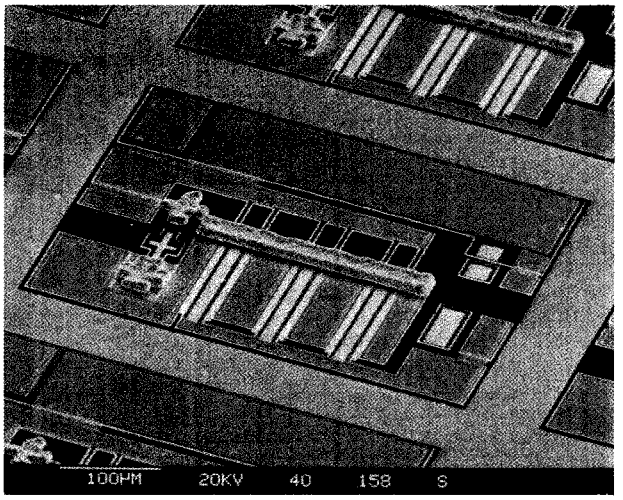

Fig. 2: SEM microphotograph of a feedback amplifier MMIC realized in DIOM technique and source over drain and gate airbridge interconnection

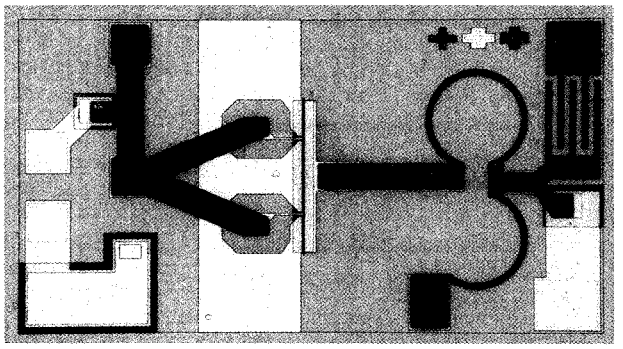

Fig. 3: SEM microphotograph of an x-band amplifier MMIC realized with lumped element input and output matching network and a 0.5 um-MESFET